Register for Certification exam

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

- Lecture 23: Processor Memory Interaction
- Lecture 24: Static and Dynamic RAM
- Lecture 25: Asynchronous DRAM
- Lecture 26: Synchronous DRAM

Week 5 : Assignment 5

Your last recorded submission was on 2021-08-30, 12:09 IST

Due date: 2021-09-01, 23:59 IST.

1) Which of the following statement(s) is/are true? *1 point*

a. In memory, data are stored in the form of 0's and 1's.
b. Memory system stores data and instruction.
c. Every bit of memory has a unique address.
d. All of these

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.

2) Consider a memory with "n" address line and "m" data lines what will be the total number of bits in the memory. *1 point*

a. $2^m \times n$
b. $2^n \times m$
c. 2^{n+m}
d. $m^2 \times n$

- ( ) a.
- (•) b.
- ( ) c.
- ( ) d.

Lecture 27: Memory Interfacing and Addressing
Week 5 Lecture Material
Quiz: Week 5 : Assignment 5
Feedback form for Week 5
Week 6
DOWNLOAD VIDEOS
Assignments Solution

3) Which of the following statement(s) is/are false? *1 point*

a. In volatile memory data is lost when power is switched off.
b. Dynamic memory requires periodic refreshing.
c. Magnetic tape does not allow random access of data.
d. None of these.

- [ ] a.
- [ ] b.
- [ ] c.
- [x] d.

4) What is/are false for cache memory? *1 point*

a. It consumes low power as compared to main memory.
b. It is a type of non-volatile memory.
c. It decrease the effective speed of the memory system.
d. All of these.

- [ ] a.
- [x] b.
- [x] c.
- [ ] d.

5) The total number of external connection required by an 8 x 8 memory will be _____?

15

1 point

6) Which of the following is/are true for virtual memory system? *1 point*

a. It increases the size of the program that can be run
b. It increases the size of the physical memory
c. It increases the size of the secondary memory
d. It improves the processor-memory bandwidth

- [x] a.
- [x] b.
- [ ] c.
- [ ] d.

7) Which of the following statement is true for writing 1 in SRAM chip? *1 point*

a. The bit line b is set with 1, and bit line b' is set with 0.
b. The bit line b is set with 0, and bit line b' is set with 1.
c. The bit line b is set with 1, and bit line b' is set with 1.
d. The bit line b is set with 0, and bit line b' is set with 0.

- (●) a.
- ( ) b.
- ( ) c.
- ( ) d.

8) Consider a 1Mbit memory organized as 1024 (rows) and 1024 (columns). If the data bus is 16-bit wide, total number of address lines required will be: *1 point*

a. 16
b. 14
c. 15
d. 20

- (●) a.
- ( ) b.
- ( ) c.
- ( ) d.

9) For a DDR2 SDRAM if the internal clock is 140MHz and bus clock is 350MHz, what will be the maximum data transfer rate? *1 point*

a. 4.48 KB/s
b. 4.48 MB/s
c. 4.48 GB/s
d. 4.48 TB/s

- ( ) a.
- ( ) b.
- (●) c.
- ( ) d.

10) Consider a memory chip with size 1 Gbyte. Four such chips are connected together to build a larger byte-oriented memory system using memory interleaving, where the processor data lines are 32-bits wide. If we name the four chips as M0, M1, M2 and M3, to which memory modules will the memory addresses **0542364AH** and **1A54200CH** map to?

1 point

a. M2 and M3
b. M2 and M0
c. M0 and M0
d. M0 and M1

- ○ a.
- ◉ b.
- ○ c.
- ○ d.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

All the answers are confirmed from our side if anybody have doubt in any of these question kindly contact us

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